REMARKS

The Office Action mailed July 24, 2001, has been received and reviewed. Claims 25, 26, 31-34, 37-40, and 43-49 are currently pending in the application. Claims 25, 26, 31-34, 37-40, and 43-49 stand rejected. Applicants request clarification as to whether the Supplemental Response mailed on July 5, 2001, overcame the Notice of Non-Compliant Amendment mailed with the Office Action of June 14, 2001. Applicants have amended claims 25, 33, 39, and 46 and respectfully request reconsideration of the application as amended herein.

35 U.S.C. § 132 Objection to the Amendment of November 28, 2000

Applicants' Amendment of November 28, 2000, has been objected to under 35 U.S.C. § 132 as introducing new matter into the disclosure. The examiner states that the term "free of field oxide structures" is not supported by the original disclosure. Applicants respectfully submit that new matter has not been introduced into the disclosure and that amending the claims to include the limitation "free of field oxide structures" is entirely appropriate.

While the addition of new matter is prohibited, any "information contained in any one of the specification, claims, or drawings of the application as filed may be added to any other part of the application without introducing new matter." M.P.E.P. § 2163.06. In addition, M.P.E.P. § 2163.07(a) states that "[b]y disclosing in a patent application a device that inherently . . . has a property, . . . a patent application necessarily discloses that . . . [property], even though it says nothing explicit concerning it. The application may later be amended to recite the . . . [property] without introducing prohibited new matter."

The term "free of field oxide structures" is fully supported by the as-filed application because the application discloses that the pre-anneal intermediate structure is inherently free of field oxide structures. Specifically, the as-filed application discloses that the field oxide structures are formed only after a substantially dopant-free, uninterrupted diffusion barrier layer is deposited on both surfaces of the semiconductor surface and is subsequently annealed. Page 8, line 27-page 9, line 4; FIGs. 7-8. As is best shown by comparing FIGs. 1-3 with FIGs. 7-8, these

field oxide structures are not present before the semiconductor substrate has been annealed. Since the as-filed application discloses that the field oxide structures are not present before annealing, the pre-anneal intermediate structure is inherently "free of field oxide structures." Therefore, the original disclosure supports this limitation and it is not new matter.

35 U.S.C. § 112 Claim Rejections

35 U.S.C. § 112, ¶1 Rejections

Claims 25, 26, 31-34, 37-40, and 43-49 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter that was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The examiner states that the term "free of field oxide [structures]" was not found in the as-filed application and that there is no written description of the term. Office Action of July 24, 2001, pages 2 and 11. Applicants respectfully traverse this rejection, as hereinafter set forth.

The as-filed application discloses that the field oxide is grown on the semiconductor substrate after the semiconductor has been doped and annealed. Page 8, lines 27-28; FIG. 7. Subsequently, portions of the field oxide are removed, resulting in the formation of a field isolation structure. Page 9, lines 2-4; FIG. 8. Since the field oxide is only grown after the annealing step, the field oxide is not present on the pre-anneal intermediate structure. In other words, the pre-anneal intermediate structure lacks field oxide structures and, therefore, is inherently "free of field oxide structures."

In light of these arguments, Applicants respectfully submit that the § 112, ¶1 rejection of claims 25, 26, 31-34, 37-40, and 43-49 be withdrawn.

35 U.S.C. § 112,¶2 Rejections

Claims 25, 26, 31-34, 37-40, and 43-49 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject

matter which Applicants regard as the invention. The examiner states that Applicants are attempting to claim the invention by excluding what they did not invent rather than distinctly and particularly pointing out what they did invent. Applicants respectfully traverse this rejection, as hereinafter set forth.

"[T]here is nothing inherently ambiguous or uncertain about a negative limitation. So long as the boundaries of the patent protection are definitely set forth definitely, albeit negatively, the claim complies with the requirements of 35 U.S.C. 112, second paragraph." M.P.E.P. § 2173.05(i). While a negative limitation must have basis in the original disclosure, the "lack of literal basis in the specification for a negative limitation may not be sufficient to establish a *prima facie* case for lack of descriptive support." M.P.E.P. § 2173.05(i).

As discussed previously, the as-filed application discloses that the field oxide structures are not present on the pre-anneal intermediate structure because the field oxide structures are not formed until after that structure has been annealed. See FIGs. 1-3 and FIGs. 7-8. Since the application discloses that the pre-anneal intermediate structure includes a semiconductor substrate that lacks or is free of field oxide structures, the negative limitation of "free of field oxide structures" has basis in the original disclosure.

Applicants respectfully submit that, in light of these arguments, the § 112, ¶2 rejections of claims 25, 26, 31-34, 37-40, and 43-49 be withdrawn.

35 U.S.C. § 103(a) Obviousness Rejections

Claims 25, 26, 31-34, 37-40, and 43-49 stand rejected under 35 U.S.C. § 103(a) ("Section 103") as being unpatentable over one of various combinations of U.S. Patent No. 5,545,577 issued to Tada ("Tada"), U.S. Patent No. 5,874,325 issued to Koike ("Koike"), and U.S. Patent No. 5,846,596 issued to Shim et al. ("Shim"). Applicants respectfully submit that none of the combinations of references cited in the Office Action of July 24, 2001, establish a *prima facie* case of obviousness.

M.P.E.P. § 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. **First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings.** Second, there must be a reasonable expectation of success. **Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) (emphasis added).

The examiner bears the burden of establishing that each of these three criteria has been met. If one of these criteria is not met, a *prima facie* case of obviousness has not been established.

Obviousness Rejection of Claims 25, 26, and 31 Based on Tada in View of Koike

Claims 25, 26, and 31 stand rejected under Section 103 as being unpatentable over Tada in view of Koike. Applicants respectfully submit that the rejection of claims 25, 26, and 31 is improper for two reasons. First, there is no suggestion or motivation to combine the references to produce the claimed invention. Second, Tada and Kioke do not teach or suggest all the claim limitations.

As amended, independent claim 25 recites a pre-anneal intermediate structure in the formation of an isolation structure that, among other things, includes a semiconductor substrate that is free of field oxide structures and has first and second opposing surfaces. The pre-anneal intermediate structure also has a substantially dopant-free, uninterrupted diffusion barrier layer extending over both the first and second surfaces of the semiconductor. This diffusion barrier layer is of sufficient depth to substantially reduce encroachment of an isolation structure formed after the pre-anneal intermediate structure has been annealed.

First, there is no motivation to combine Tada and Kioke to produce the claimed invention. The examiner asserts that it would have been obvious to combine Tada and Kioke to prevent oxidation of the second surface in Tada. However, "the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also

suggests the desirability of the combination." M.P.E.P. § 2143.01; *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990) (emphasis added). Furthermore, the fact that the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references. *Ex parte Levengood*, 28 U.S.P.Q.2d 1300 (Bd. Pat. App. & Inter. 1993).

As acknowledged by the examiner, Tada does not disclose a substantially dopant-free, uninterrupted barrier layer that extends over the second surface of the substrate. Office Action of July 24, 2001, page 4. Rather, Tada discloses a method of producing a semiconductor device that has two MIS transistor circuits on a first surface of the device. A silicon nitride layer is used as a mask to form a field oxide film on the first surface of the semiconductor substrate. Column 6, lines 27-31. As a result, gate oxides of different thicknesses are produced without contacting the resist layer, thus reducing contamination due to the resist. Column 8, line 48-column 9, line 9.

Kioke discloses a method of manufacturing a semiconductor device that includes a gettering layer. The gettering layer is comprised of a silicon thin film to which impurities have been added. Column 1, lines 53-56. The silicon thin film is applied to both surfaces of a semiconductor substrate. Column 6, line 56-column 7, line 2. Silicon nitride layers are then deposited over the silicon thin films to protect the gettering properties of the silicon thin film layers until the manufacturing process is complete. Column 6, line 56-Column 7, line 25.

While Kioke discloses a substantially dopant-free, uninterrupted barrier layer that extends over both surfaces of the substrate, neither Tada nor Kioke provide any motivation or suggestion to combine their teachings to produce the invention recited in claim 25. Nothing disclosed in Tada suggests the desirability of its second surface having a substantially dopant-free, uninterrupted barrier layer. In addition, while Kioke disclosed using the silicon nitride layer on both surfaces to protect the gettering properties of the underlying layers, it does not suggest the desirability of forming silicon nitride layers on both surfaces of other semiconductor substrates,

such as the substrate disclosed in Tada. The examiner has also not provided an objective reason to combine the references. While the examiner asserts that the motivation is to prevent oxidation of the second surface of the substrate, the claimed invention discloses that the substantially dopant-free, uninterrupted diffusion barrier layer is applied to reduce encroachment of isolation structures, not to prevent oxidation.

Second, Tada and Kioke do not teach or suggest all the claim limitations of claim 25 as amended. Specifically, Tada and Kioke do not teach or suggest "a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface of said semiconductor substrate, wherein said substantially dopant-free, uninterrupted diffusion barrier layer is a sufficient depth to substantially reduce encroachment of said isolation structure formed after annealing of said pre-anneal intermediate structure" because they do not teach or suggest that their silicon nitride layers substantially reduce encroachment of isolation structures.

As discussed previously, Tada uses its silicon nitride layer as a mask to form a field oxide film on the first surface of its semiconductor substrate. Kioke uses its silicon nitride layers to protect the underlying silicon thin films layers that act as gettering layers. Neither of the references teach or suggest that their silicon nitride layers reduce encroachment of isolation structures or even address the problem of isolation structure encroachment.

Applicants respectfully submit that a *prima facie* case of obviousness of claim 25 has not been established because there is no motivation or suggestion to combine the references and because the references do not disclose all the claim limitations. Therefore, Applicants respectfully request that the rejection of claim 25 be withdrawn.

Dependent claims 26 and 31 include all of the claim limitations of claim 25 and, therefore, are allowable as depending from an allowable claim.

Obviousness Rejection of Claim 32 Based on Tada and Koike, and Further in View of Shim

Claim 32 stands rejected under Section 103 as being unpatentable over Tada and Koike, as applied to claim 25 above, and further in view of Shim. Applicants respectfully traverse this rejection, as hereinafter set forth.

Since claim 32 depends from claim 25, it includes all the claim limitations of claim 25. Claim 32 recites a pre-anneal intermediate structure that includes, among other things, a semiconductor substrate that is free of field oxide structures and has first and second opposing surfaces. The pre-anneal intermediate structure also includes a substantially dopant-free, uninterrupted diffusion barrier layer extending over both the first and second surfaces of the semiconductor. This diffusion barrier layer is comprised of silicon oxynitride and is of sufficient depth to substantially reduce encroachment of an isolation structure formed after the pre-anneal intermediate structure has been annealed.

As discussed above in the Section 103 rejection of claim 25, there is no motivation to combine Tada and Koike because those references do not suggest that silicon nitride layers should be formed over both surfaces of a semiconductor substrate to produce the claimed invention. Applicants further submit that Shim does not provide this motivation or suggestion.

Shim discloses a method of forming field oxide isolation regions having sloped edges. Column 2, lines 5-6. In this method, a silicon nitride or silicon oxynitride layer is applied to one surface of a substrate and is used as a first oxidation resistant layer. Column 3, lines 17-19. The first oxidation resistant layer, in combination with a first pad insulation layer, is patterned to expose portions of the substrate, which are subsequently oxidized into field oxide isolation regions having sloped walls. Column 3, lines 19-67. Nothing in Shim discloses that the first oxidation resistant layer should be formed on both surfaces of the semiconductor substrate. Therefore, Shim does not provide the requisite motivation or suggestion to combine the cited references to produce the claimed invention.

In addition, Shim does not teach or suggest the claim limitation of "a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said

second surface of said semiconductor substrate, wherein said substantially dopant-free, uninterrupted diffusion barrier layer is a sufficient depth to substantially reduce encroachment of said isolation structure formed after annealing of said pre-anneal intermediate structure." Rather, Shim uses its silicon nitride layer, which is deposited on one surface of the substrate, as a mask layer.

Finally, the nonobviousness of independent claim 25 precludes the rejection of claim 32 because a dependent claim is obvious only if the independent claim from which it depends is obvious. *See In re Fine,* 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988); *see also* M.P.E.P. § 2143.03.

Since a *prima facie* case of obviousness has not been established for the reasons discussed above, Applicants respectfully submit that the rejection of claim 32 be withdrawn.

Obviousness Rejection of Claims 33, 34, 37, and 38 Based on Tada in View of Koike

Claims 33, 34, 37, and 38 stand rejected under Section 103 as being unpatentable over Tada in view of Koike. Applicants respectfully submit that the rejection of claims 33, 34, 37, and 38 is improper for two reasons. First, there is no suggestion or motivation to combine the references to produce the claimed invention. Second, Tada and Kioke do not teach or suggest all the claim limitations.

Claim 33 recites a pre-anneal intermediate structure in the formation of an isolation structure for a semiconductor device. The pre-anneal intermediate structure includes a semiconductor substrate that is free of field oxide structures and has first and second opposing surfaces. The pre-anneal intermediate structure also has a substantially dopant-free, uninterrupted diffusion barrier layer extending over both the first and second surfaces of the semiconductor. This diffusion barrier layer is of sufficient depth to substantially reduce encroachment of an isolation structure formed after the pre-anneal intermediate structure has been annealed.

First, there is no suggestion or motivation to combine Tada and Kioke for the same reasons discussed above in the Section 103 rejection of claims 25, 26, and 31.

Second, Tada and Kioke do not teach or suggest all the claim limitations of claim 33. Specifically, Tada and Kioke do not teach or suggest "a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface of said semiconductor substrate, wherein said substantially dopant-free, uninterrupted diffusion barrier layer is a sufficient depth to substantially reduce encroachment of said isolation structure formed after annealing of said pre-anneal intermediate structure" for the same reasons discussed above in the Section 103 rejection of claims 25, 26, and 31.

For the reasons discussed above, Applicants respectfully submit that a *prima facie* case of obviousness of claim 33 has not been established because there is no motivation or suggestion to combine the references and because the references do not disclose all the claim limitations. Therefore, Applicants respectfully request that the obviousness rejection of claim 33 be withdrawn.

Dependent claims 34, 37, and 38 include all of the claim limitations of claim 33 and, therefore, are allowable as depending from an allowable claim.

Obviousness Rejection of Claims 39, 40, and 43-45 Based on Tada in View of Koike

Claims 39, 40, and 43-45 stand rejected under Section 103 as being unpatentable over Tada in view of Koike. Applicants respectfully submit that the rejection of claims 39, 40, and 43-45 is improper for two reasons. First, there is no suggestion or motivation to combine the references to produce the claimed invention. Second, Tada and Kioke do not teach or suggest all the claim limitations.

Claim 39 recites a pre-anneal intermediate structure in the formation of an isolation structure for a semiconductor device. The pre-anneal intermediate structure includes a semiconductor substrate that is free of field oxide structures and has first and second opposing surfaces. The pre-anneal intermediate structure also has a substantially dopant-free, uninterrupted diffusion barrier layer extending over both the first and second surfaces of the semiconductor. This diffusion barrier layer is of sufficient depth to substantially reduce

encroachment of an isolation structure formed after the pre-anneal intermediate structure has been annealed.

First, there is no suggestion or motivation to combine Tada and Kioke for the same reasons discussed above in the Section 103 rejection of claims 25, 26, and 31.

Second, Tada and Kioke do not teach or suggest all the claim limitations of claim 39. Specifically, Tada and Kioke do not teach or suggest "a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface of said semiconductor substrate, wherein said substantially dopant-free, uninterrupted diffusion barrier layer is a sufficient depth to substantially reduce encroachment of said isolation structure formed after annealing of said pre-anneal intermediate structure," for the same reasons discussed above in the Section 103 rejection of claims 25, 26, and 31.

For the reasons discussed above, Applicants respectfully submit that a *prima facie* case of obviousness of claim 39 has not been established because there is no motivation or suggestion to combine the references and because the references do not disclose all the claim limitations. Therefore, Applicants respectfully request that the obviousness rejection of claim 39 be withdrawn.

Dependent claims 40 and 43-45 include all of the claim limitations of claim 39 and, therefore, are allowable as depending from an allowable claim.

Obviousness Rejection of Claims 46-48 Based Tada in View of Koike

Claims 46-48 stand rejected under Section 103 as being unpatentable over Tada in view of Koike. Applicants respectfully submit that the rejection of claims 46-48 is improper for two reasons. First, there is no suggestion or motivation to combine the references to produce the claimed invention. Second, Tada and Kioke do not teach or suggest all the claim limitations.

Claim 46 recites a pre-anneal intermediate structure useful in the formation of electrical device isolation structures. The pre-anneal intermediate structure includes a semiconductor substrate that is free of field oxide structures and has first and second opposing surfaces. The

pre-anneal intermediate structure also has a substantially dopant-free, uninterrupted diffusion barrier layer extending over both the first and second surfaces of the semiconductor substrate, thereby encapsulating the semiconductor substrate. This diffusion barrier layer is of sufficient depth to substantially reduce encroachment of an isolation structure formed after the pre-anneal intermediate structure has been annealed.

First, there is no suggestion or motivation to combine Tada and Kioke for the same reasons discussed above in the Section 103 rejection of claims 25, 26, and 31.

Second, Tada and Kioke do not teach or suggest the claim limitation of "a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface of said semiconductor substrate, wherein said substantially dopant-free, uninterrupted diffusion barrier layer is a sufficient depth to substantially reduce encroachment of said isolation structure formed after annealing of said pre-anneal intermediate structure," for the same reasons discussed above in the Section 103 rejection of claims 25, 26, and 31.

For the reasons discussed above, Applicants respectfully submit that a *prima facie* case of obviousness of claim 46 has not been established because there is no motivation or suggestion to combine the references and because the references do not disclose all the claim limitations. Therefore, Applicants respectfully request that the obviousness rejection of claim 46 be withdrawn.

Dependent claims 47 and 48 include all of the claim limitations of claim 46 and, therefore, are allowable as depending from an allowable claim.

Obviousness Rejection of Claim 49 Based on Tada and Koike and Further in View of Shim

Claim 49 stands rejected under Section 103 as being unpatentable over Tada and Koike in view of Shim. Applicants respectfully traverse this rejection, as hereinafter set forth.

Since claim 49 depends from claim 46, it includes all the claim limitations of claim 46. Claim 49 recites a pre-anneal intermediate structure useful in the formation of electrical device isolation structures. The pre-anneal intermediate structure includes, among other things, a

semiconductor substrate that is free of field oxide structures and has first and second opposing surfaces. The pre-anneal intermediate structure also includes a substantially dopant-free, uninterrupted diffusion barrier layer extending over both the first and second surfaces of the semiconductor substrate, thereby encapsulating the semiconductor substrate. This diffusion barrier layer is comprised of silicon oxynitride and is of sufficient depth to substantially reduce encroachment of an isolation structure formed after the pre-anneal intermediate structure has been annealed.

Claim 49 is not obvious for the same reasons discussed above in the Section 103 rejection of claim 32. In summary, first, there is no motivation to combine the references. Second, the references do not teach or suggest all the claim limitations. Finally, the nonobviousness of independent claim 46 precludes the rejection of claim 49, which depends from claim 46, because a dependent claim is obvious only if the independent claim from which it depends is obvious. *See In re Fine,* 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988); *see also* M.P.E.P. § 2143.03.

Since a *prima facie* case of obviousness has not been established for the reasons discussed above, Applicants respectfully submit that the rejection of claim 49 be withdrawn.

In conclusion, Applicants respectfully submit that the Section 103 rejections of claims 25, 26, 31-34, 37-40, and 43-49 should be withdrawn because the cited references do not establish a *prima facie* case of obviousness for two reasons. First, there is no motivation or suggestion to combine the references to produce the claimed invention. Second, the cited references do not teach or suggest all the claim limitations.

Drawings

Applicants submit herewith corrected formal drawings, under cover of a separate Transmittal of Formal Drawings. Applicants respectfully request approval of the corrected formal drawings.

ENTRY OF AMENDMENTS

The amendments to claims 25, 33, 39, and 46 should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application.

CONCLUSION

Claims 25, 26, 31-34, 37-40, and 43-49 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

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Enclosure: Version With Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

device claim

25. (Five times amended) A pre-anneal intermediate structure in the formation of an isolation structure for a semiconductor device, comprising:

a semiconductor substrate free of field oxide structures and having a first surface and a second surface, said first surface opposing said second surface;

at least one p-well and at least one n-well on said substrate first surface;

at least one p-type area within said at least one n-well;

at least one n-type area within said at least one p-well; and

a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface of said semiconductor substrate, wherein said substantially dopant-free, uninterrupted diffusion barrier layer is a sufficient depth to substantially reduce encroachment of said isolation structure formed after annealing of said pre-anneal intermediate structure.

33. (Three times amended) A pre-anneal intermediate structure in the formation of an isolation structure for a semiconductor device, comprising:

a semiconductor substrate free of field oxide structures and having a first surface and a second surface, said first surface opposing said second surface;

at least one p-well and at least one n-well on said substrate first surface;

at least one doped area within at least one of said at least one n-well and said at least one p-well; and

a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface of said semiconductor substrate, wherein said substantially dopant-free, uninterrupted diffusion barrier layer is a sufficient depth to substantially reduce encroachment of said isolation structure formed after annealing of said pre-anneal intermediate structure.

39. (Three times amended) A pre-anneal intermediate structure in the formation of an isolation structure for a semiconductor device, comprising:

a semiconductor substrate free of field oxide structures and having a first surface and a second surface, said first surface opposing said second surface;

at least one first doped area on said substrate first surface;

at least one second, differently doped area within said at least one first doped area; and

a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface of said semiconductor substrate, wherein said substantially dopant-free, uninterrupted diffusion barrier layer is a sufficient depth to substantially reduce encroachment of said isolation structure formed after annealing of said pre-anneal intermediate structure.

46. (Amended) A pre-anneal intermediate structure useful in the formation of electrical device isolation structures, comprising:

a semiconductor substrate that is free of field oxide structures and includes a first surface and a second surface, said first surface opposing said second surface;

at least one p-well and at least one n-well defined on said first surface of said substrate;

at least one p-type area defined within said at least one n-well;

at least one n-type area defined within said at least one p-well; and

a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface, said substantially dopant-free, uninterrupted diffusion barrier layer encapsulating said semiconductor substrate, wherein said substantially dopant-free, uninterrupted diffusion barrier layer is a sufficient depth to substantially reduce encroachment of said isolation structure formed after annealing of said pre-anneal intermediate structure.